21. (New) The system of claim 1, wherein:

the cache memory can simultaneously hold multiple non-consecutive quadwords.

22. (New) The system of claim 1, wherein:

the cache memory comprises an address cache and a data cache.

23. (New) The apparatus of claim 6, wherein:

the cache memory can simultaneously hold multiple non-consecutive quadwords.

24. (New) The apparatus of claim 6, wherein:

the cache memory comprises an address cache and a data cache.

REMARKS

Claim 11 has been objected to for lack of antecedent basis. Claim 11 has been cancelled, rendering the rejection moot.

Claims 1-3, 6-8, 10-11 and 15 have been rejected under 35 USC 102(e) as being anticipated by U.S. patent no. 6,263,398 ("Taylor").

Claim 5 has been rejected under 35 USC 103(a) as being unpatentable over U.S. patent no. 6,288,923 ("Sakamoto") in view of Taylor.

Claims 16-18 have been rejected under 35 USC 103(a) as being unpatentable over Sakamoto in view of admitted prior art.

Claim 19 has been rejected under 35 USC 103(a) as being unpatentable over U.S. Sakamoto in view of Taylor and admitted prior art.

Claims 4, 9, and 14 have been rejected under 35 USC 103(a) as being unpatentable over Sakamoto in view of U.S. patent no. 6,347,055 ("Motomura"), or alternatively over Taylor in view of Motomura.

Claim 20 has been rejected under 35 USC 103(a) as being unpatentable over Sakamoto in view of admitted prior art and Motomura.

Applicants respectfully traverse these rejections because the cited references do not disclose or suggest every element of any claim, as the following analysis shows.

Claims 10-20 have been cancelled, rendering the rejections to those claims moot. Independent claims 1 and 6 recite that the cache memory stores data from non-consecutive addresses. Support for this limitation may be found in the specification in paragraph 0028. Taylor does not disclose this limitation. Taylor teaches against this limitation by designing a cache memory that holds only a single row (page) of data, requiring that the entire cache be occupied by only that pre-defined block of consecutively-addressed data. This design is discussed throughout the Taylor reference, with repeated references to "in page" reads (e.g., col. 3 line 25) and by defining the cache as a register that holds only the last row read (col. 5 lines 9). Taylor defines a page as a row (col. 8 lines 31, 45), thus confining his cache to the size of a row, which is hardwired into the main memory array. With these design constraints, the design of Taylor could not even be feasibly modified to include data from non-consecutive addresses.

Claims 2-5, 21, 22 depend from claim 1, while claims 7-9, 23, 24 depend from claim 6, and these claims therefore contain the same limitations not disclosed or suggested by the cited references.

In addition, claim 5 recites that the processor is in the same integrated circuit as the cache and main memories. Taylor does not disclose this limitation.

In addition, claims 21, 23 recite that the cache holds non-consecutive quadwords. Support for this limitation may be found in the specification in paragraph 0028. Taylor does not discuss quadwords, and instead limits his cache to holding only a page of consecutively addressed data defined by the row/column architecture of the main memory device.

In addition, claims 22, 24 recite that the cache comprises both an address cache and a data cache. Support for this limitation may be found in Fig. 4 and in the specification in paragraph 0024. Taylor does not disclose this.

The Sakamoto and Motomura references and the admitted prior art do not disclose or suggest the aforementioned limitations that are missing from Taylor.

CONCLUSION

For the foregoing reasons, Applicant submits that claims 1-9 and 21-24 are now in condition for allowance, and indication of allowance by the Examiner is respectfully requested. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as

possible. No fee is believed due in connection with this response. If this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOLOKOFF, TAYLOR & ZAFMAN, LLP

Date: 12-04-02

John Travis
Reg. No. 43,203

12400 Wilshire Blvd
Seventh Floor
Los Angeles, California 90025-1026
(512) 434-2400

APPENDIX A

Marked-up version of amended claims

1. (Amended once) A system comprising:

a processor; and

a memory device coupled to the processor and contained within a single integrated circuit, the memory device including:

a main memory; and

a cache memory coupled to the processor and to the main memory to store data from non-consecutive addresses requested from the main memory. [increase effective access speed between the processor and the memory device.]

2. (Amended once) The system of claim 1, wherein:

all circuitry to operate the cache memory is contained within the memory device.

[the cache memory and main memory are on a same integrated circuit.]

5. (Amended once) The system of claim 1, wherein:

the [cache memory, main memory, and] processor [are on a same] is contained within the single integrated circuit.

6. (Amended once) An apparatus comprising:

a memory device to couple to a processor through a bus, the memory device including on a single integrated circuit:

a main memory; and

a cache memory coupled to the main memory to store data from non-consecutive addresses requested from the main memory. [increase effective access speed between the processor and the memory device.]

7. (Amended once) The apparatus of claim 6, wherein:

all circuitry to operate the cache memory is contained within the single integrated circuit. [the cache memory is on a same integrated circuit as the main memory.]

10-20. (Cancelled)

21. (New) The system of claim 1, wherein:

the cache memory can simultaneously hold multiple non-consecutive quadwords.

22. (New) The system of claim 1, wherein:

the cache memory comprises an address cache and a data cache.

23. (New) The apparatus of claim 6, wherein:

the cache memory can simultaneously hold multiple non-consecutive quadwords.

24. (New) The apparatus of claim 6, wherein:

the cache memory comprises an address cache and a data cache.